Efficient Development of Mass Producible MMIC Circuits

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Abstract—**The state of the art criteria and tools for an efficient development of mass producible MMIC's are discussed with reference to a specific development philosophy. The available yield evaluation systems are then critically analyzed and the results are reported of a systematic functional yield evaluation we performed on a large number of monolithic circuit components. Subsequently a statistically meaningful data base (including both FET equivalent circuit and *S* parameters) is reported, that we developed for parametric yield evaluation and yield driven design centering. Finally, through a significant example, the possibility is demonstrated of drastically improving the accuracy of the parametric circuit yield forecasts by using a small set of mutually uncorrelated process dependent parameters and by making reference to a physically based semiempirical FET model.**

I. Introduction

MONOLITHIC microwave integrated circuits (MMIC's) offer, as well known [1], a number of important advantages over the more conventional hybrid circuits, such as reduced costs (especially for high volume production), higher (potential) reliability, smaller sizes and weights, inherent wide band performance and capability of performing analog and digital functions on the same chip. The impact of such advantages on the microwave industry has been so strong that many companies worldwide developed an MMIC capability [2] and a number of GaAs foundries were created for the production of customer designed MMIC's.

In spite of this success, several problems still hinder the development of high yield mass producible MMIC's [2]–[4]. This is proven by the fact that most of the MMIC prototypes developed do not reach the market and the fact that the available foundry manuals [3] do not usually give the readers adequate information for a reasonable evaluation of yield (and reliability) of a given circuit topology. A number of very interesting and scientifically valid books [4]–[8] covering MMIC technology and design tools have recently been published, but, although the concept of yield driven design centering was proposed by J. W. Bandler and, specifically for MMIC's, by R. A. Pucel several years ago [6], not much attention has been devoted to solving these problems. Before the launch of specific programs sponsored by the U.S. Department of Defence [9], yield topics were for a long time relatively neglected by the international literature, and even today the lack of a solid background of statistical data makes the validity of various recent contributions on the MMIC FET modeling statistics [10] often questionable. Moreover, papers on yield based process qualification, are usually not available in the open literature (although they are possibly known within companies involved in the MIMIC or similar programs).

The present work documents our effort for assessing a full development procedure for high yield, mass producible MMIC's. The purpose of the paper can be summarized as follows:

1) Describe and analyze a specific philosophy for the development of high yield mass producible MMIC's.
2) Outline, within the frame of point 1 description, the inadequacies of the available design tools and describe the practical solutions usually employed for overcoming these limitations.
3) Discuss the yield calculation and optimization criteria.
4) Report the results of a systematic functional yield analysis performed on a large number of MMIC components.
5) Describe and analyze the data of a statistically meaningful and selfconsistent data base for both FET equivalent circuit and *S* parameters relevant to a standard 0.5 μm MMIC process.
6) Demonstrate the possibility of predicting with good accuracy the MMIC parametric yield by using a physically based FET model, semiempirically centered on the process parameters.
7) Give data and references useful for foundry selection.

II. The Philosophy for High Yield Mass Producible MMIC Development

In spite of the fact that a modern MMIC might seem a very simple circuit, its design and optimization for high yield mass production are complex. The circuit design usually starts from the definition of the target specifications, on the basis of which a decision must be made about the convenience and the suitability of a monolithic approach. The decision must be based on the knowledge of

Manuscript received August 13, 1991; revised February 10, 1992.
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IEEE Log Number 9108321.

the individual monolithic circuit element capabilities and of the performances achieved in previously developed MMIC's.

For MMIC design the circuit elements need to be characterized by fairly complex equivalent circuits which take into account their intrinsic parasitics. For this reason an extensive use must be done of CAD tools. The equivalent circuits are often obtained through empirical fitting of precision microwave measurements made on a large number of components of different values and shapes, since the available full theoretical models do not exhibit the required accuracy [3].

A typical example of this situation is that of the polygonal spiral inductor. In fact, when modeling, for example, square spirals almost all the available CAD tools give unrealistic symmetrical outputs which do not take adequately into account the effects of the intertrack coupling and of the underpass or overpass connection (the only exception we know being [3], [6] constituted by the LINMIC+ program [2], [11]). References [12], [13] report specific cases of simple discontinuities and linear circuit elements, frequently encountered in MMIC development, where commercially available CAD programs usually give unsatisfactory results (both in terms of modeling and of computational cost). Most of the small signal active device equivalent circuits available from foundries also show weaknesses [3], [4], [6], [12], [14] such as when taking into account the difference of the low frequency and microwave output resistance and when systematically considering the dependence of the equivalent circuit parameters both on bias and on device temperature. Moreover, some suspicion exists on the high frequency validity of the lumped element equivalent circuit scaling criteria because of the distributed nature of the devices. For this reason special importance is assumed by recent efforts for providing practical distributed models based on geometrical and process parameters easily implementable in the existing CAD [15]. Large signal device models are often [3], [12] even more limited particularly because of the difficulty of accounting for avalanche mechanism and temperature rise under operation.

When a first prototype electrical design of acceptable performance has been obtained, consideration must be given to the overall chip layout and to a first rough check of the various production yields. Since the cost is strictly related to the chip area, particular attention must be paid to its minimization. This, however, increases intercomponent coupling effects. On this subject it has to be noted that proximity effects can be easily calculated for very simple geometries. The difficulty of handling sufficiently accurate single component theoretical models and the risk of undesired proximity coupling may sometimes require experimental evaluations on particular circuit subnetworks which can be included in the process test patterns or, if the quasi monolithic test approach is chosen [16], realized over low cost semiinsulating GaAs substrates.

Some iterations, and sometimes a specification review may become necessary prior to complete fulfilment of the performance and layout requirements. At this stage the previous rough yield analysis must be refined by taking into account the specifics of the layout and a yield driven design centering procedure, using reasonable performance ranges, must be made on the basis of the fabrication process tolerances. This will be considered in detail in the next paragraph.

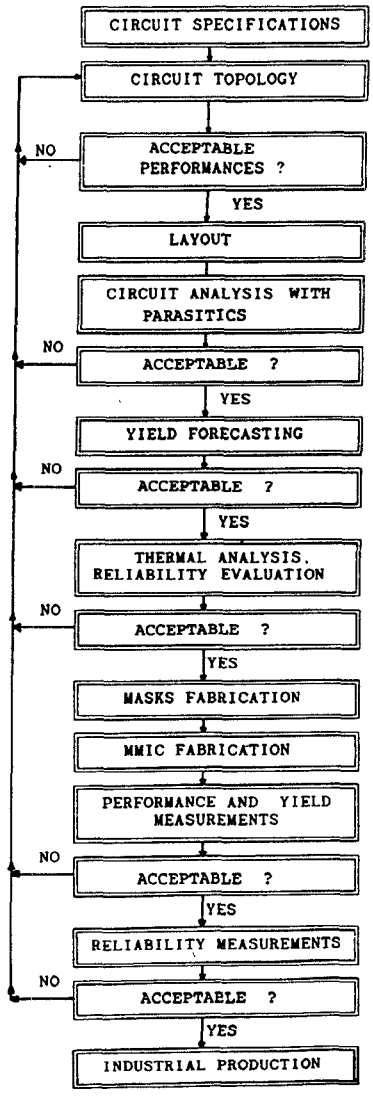

Fig. 1. Flow chart of the development process for mass producible MMIC's.

If the yield values are acceptable, the circuit can be released for fabrication of prototypes. If such prototypes comply with the revised specifications the circuit can be subjected to the subsequent development stages. Otherwise, the reasons for the unsatisfactory results must be identified: this is frequently quite a difficult task since material, processing, layout, and mask manufacturing errors can all be responsible. On the other hand an experimental fault diagnosis is difficult because of the circuit dimensions. An intelligent use of circuit simulation programs can be very helpful here. The fault correction will require full or partial design reconsideration. If the design, up to this point, can be considered successful, reliability tests must be made, which also may require some

design iterations before proceeding to the last development stages (packaging etc.). A flow chart showing the above described development process for mass producible MMIC's is shown in Fig. 1.

III. MMIC Yield Analysis and Functional Yield Results

As outlined elsewhere [3], the MMIC total yield, *Yt*, can be expressed as a function of the yields of manufacturing steps:

$$Yt = Yl * Ydc * Yp * Yd * Ya$$

Here *Yl* (line yield) gives the fraction of processed wafer having acceptable process control monitor (PCM) parameters. *Yl* strongly depends on the overall process reproducibility and represents a useful parameter for evaluating the maturity of the process being used.

Ydc (functional or dc yield) represents the fraction of on wafer chips which pass a full dc probing. This concept will be made clearer later.

Yp (parametric yield) gives the fraction of chips, passing the dc screening, which meet the RF performance tolerances.

Yd (dicing yield) gives the fraction of chips which survive after wafer dicing. πYa (assembly yield) gives the fraction of diced chips correctly assembled.

Yl depends on the PCM parameter acceptance ranges. These, for the Telettra foundry are reported in Table I. It is worth noting that these ranges compare (favourably) with those currently used in various foundries [3]. Reasonable *Yl* values using Table I data must be higher than 80%.

Ydc depends on circuit complexity and its value is the product of the dc yield of each circuit element. A common procedure to evaluate *Ydc* is to define a mean yield for each circuit element [17], [18]. This evaluation system is questionable [3] because the dc yield of components like FET's, diodes and capacitors is a function of their size. On the other hand, it can be shown that FETs, MIM capacitors and via holes are the only circuit components practically affecting the MMIC dc yield. In fact, all the other elements have such a high *Ydc* as to allow the definition of a size independent functional yield. For this reason some foundries take into account the effects of these elements by introducing a dc yield factor per unit chip area [3]. Our own experience has shown that for FET devices a dc yield per unit gate width can be correctly defined. Similarly a yield per unit MIM capacitance is adequate. For vias a yield per via is sufficient.

The above described functional yield calculation method includes the visual inspection results and corresponds to a careful consideration of the single component dc characteristics (for example a spiral inductors having short circuited tracks is not considered O.K. because it has a dc resistance different from the right one).

Table II summarizes the single element functional yield for the Telettra 0.5 μm MMIC process: these data, which were obtained after several years of process refinements and imply proper conditions on a wide number of specific design rules [3], [21], were determined by considering the results of five groups of 200 identical elements for each type of circuit component. For example, in the case of single gate FET's, 5 groups of 200 identical elements having 150, 300, 600, 1200, and 2400 μm gate widths respectively were tested.

TABLE I
0.5 μm Telettra Process PCM Parameter Acceptance Ranges

Parameter	Range
Saturation current	±15%
Transconductance	±15%
Pinchoff voltage	±20%
Gate to source capacitance	±20%
N layer sheet resistance	±20%
N^+ layer sheet resistance	±10%
Thin film resistors	±10%
MIM capacitor's capacitance	±10%

TABLE II
Mean Functional Yield of Monolithic Circuit Components for the 0.5 μm Telettra Process

Single Gate FET's (.5 μm × 1 mm gate)	.942
Dual Gate FET's (.5 μm × 1 mm gate)	.882
Via holes	.955
Air bridges	.995
Spiral inductors	.990
Interdigitated capacitors	.995
MIM capacitors (1 pF)	.992
Distributed elements	.998
Active layer resistors	.985
Thin film metal resistors	.996
Schottky diodes	.990

The parametric yield evaluation requires Monte Carlo calculations (easily available on standard circuit simulation programs) based on the fluctuations of the component equivalent circuit elements.

The most important parameters for determining *Yp* are those of the active devices. Foundry manuals often give this information in terms of mean value and standard deviation of the equivalent circuit parameters, which are obtained from fittings of *S* parameters measured in a given frequency range. This approach frequently suffers from the strictly numerical procedures employed which may lead to parameter values physically unrealizable [3], [10], [19], [20]. In other words the fitted equivalent circuit parameters can have values not physical (for example negative resistance values) or too far from those obtained by direct measurements with other methods. For this reason we consider very important use parameter extraction procedures which integrate the "warm" device *S* parameters data with those of the "cold" device [10], [19], [20], [22], [23] and with the results of other (dc, pulsed, etc.) measurements [19], [20]. The fully automated system we currently use [19] meets these requirements.

Foundry manuals usually report distinct tables for the equivalent circuit parameter statistics (on single wafer and

wafer to wafer). Reference [3] gives tables where merit evaluations for the component functional yield and for the single wafer and wafer to wafer FET equivalent circuit parameter variations can help the reader for a correct foundry selection and use.

Another basic limitation in the *Yp* evaluation comes from the fact that the equivalent circuit parameters are correlated with each other, while no information on their correlation is often given by the foundries. For this reason and for the fact that the correlations between the FET *S* parameters are not completely lost [10] when considering as uncorrelated the equivalent circuit data, the parametric yield calculations are frequently made under this assumption [3].

Our MMIC development and testing experience has shown that *Yp* values obtained with this procedure are not realistic. The same occurs when using correlation matrices between parameters extracted only from hot FET *S* parameter measurements. Moreover it has been noticed that if the scattering parameter data base is not sufficiently large and does exhibit bimodal type distributions [10] the obtained equivalent circuit parameter statistics may fail in reconstructing the original scattering matrix statistics [24].

In order to correct this situation Purviance *et al.* [25] proposed an approach, called the "truth model" where a statistical model for each equivalent circuit parameter is not constructed. Experimental evidence of the truth model use has been given recently. However, because of its ability to give a physical explanation of the observed phenomena and of its intrinsic flexibility when used for design purposes, the microwave community is reluctant to abandon the equivalent circuit approach (to which great efforts have been directed in the past [3], [10]). This idea has been recently reinforced by the results of Bandler *et al.* [26] who have shown that a physically based FET model [5] can closely reproduce the distribution (but not the mean values) of the measured FET scattering parameters.

The experimental results we report later prove that very accurate parametric yield evaluations can be obtained by the use of a semiempirical physically based FET model which permits a readjustment of the deterministic shift [26] in the *S* parameter mean values. This approach allows the use of a small set of really uncorrelated process related variables (like for example doping level, gate length, gate to source spacing etc.) which can be easily measured or evaluated by the MMIC manufacturers. This idea was originally suggested by Ladbrooke [27]. A final drawback of the yield driven design centering procedures we wish to outline is the long simulation times required by the use of Monte Carlo analysis into the optimization loop. For this reason particular attention has been dedicated by several recent works to speeding up the optimization algorithms [28]–[32].

We believe that the parametric yield for mass producible MMIC circuits must reasonably be higher than 90%. This proves the great design importance of the functional yield data, which however are rarely available from foundries and MMIC manufacturers. These data are very helpful when studying the feasibility of mass producible MMIC's.

Reasonable *Yd* values, for chip areas lower than 16 mm^2, must be higher than 95%. Similarly, for circuits having up to 16 pads, *Ya* must be higher than 95%.

IV. The Test MMIC and Parametric Yield Results

Going now to the point 6 of the introduction, let us consider the yield results of a test circuit: a 4–8 GHz amplifier for high capacity radio links, which has been produced for over two years at Telettra.

The circuit target specifications were:

bandwidth 4–8 GHz,
gain >10 dB,
noise figure <6 dB,
input/output reflection coefficients <-10 dB,
1 dB compression point >18 dBm,
power consumption <500 mW.

Use of one single bias voltage was also requested. In spite of the broad band allowed, a single stage feedback topology [3], [33], [34] was discarded because of the required gain level. A cascade of two inverters with resistive feedback was then chosen, which permits a better overall isolation and separate adjustments of the input/output matching conditions [35], [36]. The resulting circuit topology (Fig. 2) can be considered [6] as representative of the state of the art MMIC's developed through foundries moreover it allows the achievement of relatively reproducible performances also when process with no particularly stringent tolerances are used (see Table I). The experimentally obtained average circuit yields were:

$$Ydc = 55.1\%, \quad Yp = 91\%,$$
$$Yd = 98.5\% \quad \text{and} \quad Ya = 98\%.$$

The functional yield, calculated from Table II, data was $Ydc = 54.2\%$, in very good agreement with the experiment. For *Yp* evaluation systematic FET "hot" and "cold" FET *S* parameter measurements were made in the 1 to 18 GHz band. From these and other (pulsed) measurements [19] the device equivalent circuit parameter were deduced. On the other hand, a physically based semiempirical FET model, here described in the appendix, was developed.

Figs. 3 to 10 give (vertical segments) the experimental 10 GHz *S* parameter probability density histograms deduced from on wafer testing of 2300 0.5 * 300 μm FET's which were fabricated on 200 different wafers. No bimodal distributions were noticed on these data.

From this information the FET equivalent circuit (see Fig. 11) parameter distributions given (again vertical segments) in Figs. 12–21 were deduced. The FET *S* and equivalent circuit parameter distributions calculated (2.6E6 trials) from the device model in the appendix are also given in figures from 2 to 21 (rectangles). These re-

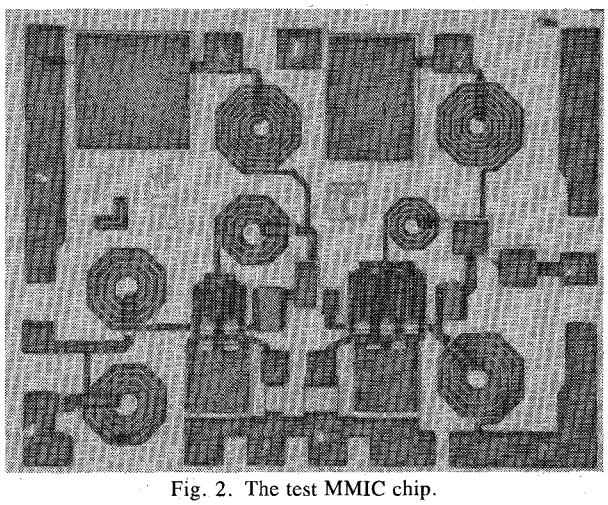

Fig. 2. The test MMIC chip.

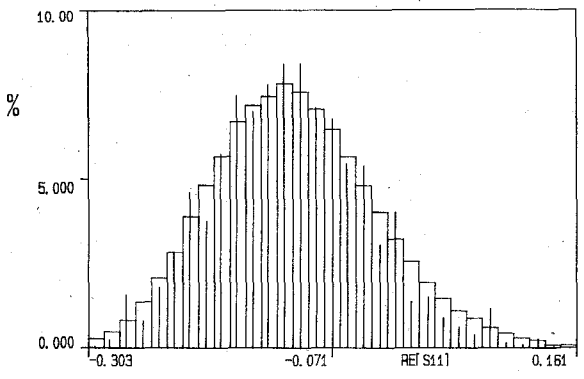

Fig. 3. Measured (vertical segments) and modeled (rectangles) histograms of the real part of $S11$ for a 300 μm wide FET device (Vds = 5 V Ids = $Idss/2$).

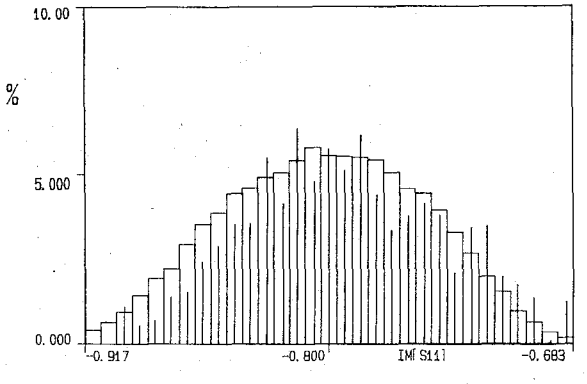

Fig. 4. Measured (vertical segments) and modeled (rectangles) histograms of the imaginary part of $S11$ for a 300 μm wide FET device (Vds = 5 V Ids = $Idss/2$).

sults were obtained by just semiempirically centering the mean values of the modeled single equivalent circuit elements on the experimental ones.

It is interesting to note that all the modeled probability density functions very well agree with the experiment, the discrepancies being of the same order of magnitude of those obtainable from the model by reducing the trial number to 2300. The test circuit parametric yield, if calculated on the basis of the above electrical specifications and of the experimental equivalent circuit parameters,

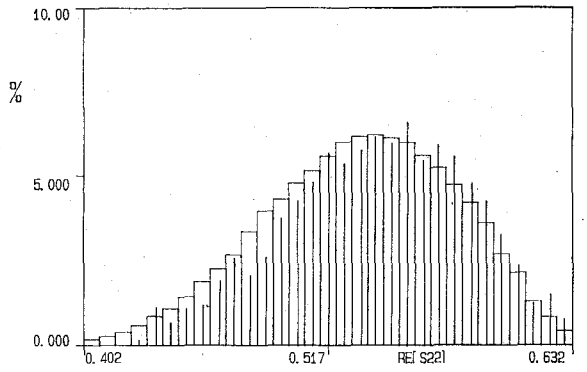

Fig. 5. Measured (vertical segments) and modeled (rectangles) histograms of the real part of $S22$ for a 300 μm wide FET device (Vds = 5 V Ids = $Idss/2$).

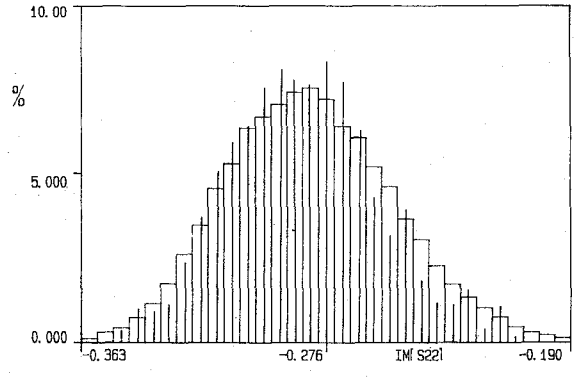

Fig. 6. Measured (vertical segments) and modeled (rectangles) histograms of the imaginary part of $S22$ for a 300 μm wide FET device (Vds = 5 V Ids = $Idss/2$).

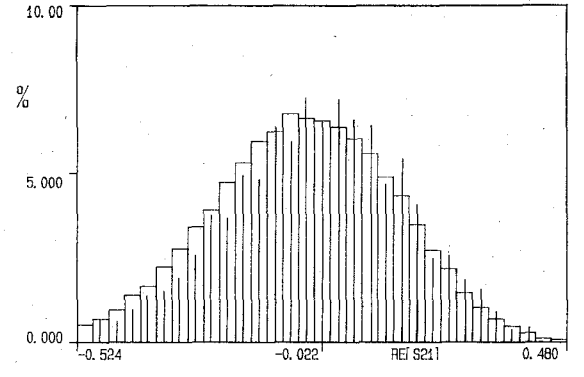

Fig. 7. Measured (vertical segments) and modeled (rectangles) histograms of the real part of S21 for a 300 μm wide FET device (Vds = 5 V Ids = $Idss/2$).

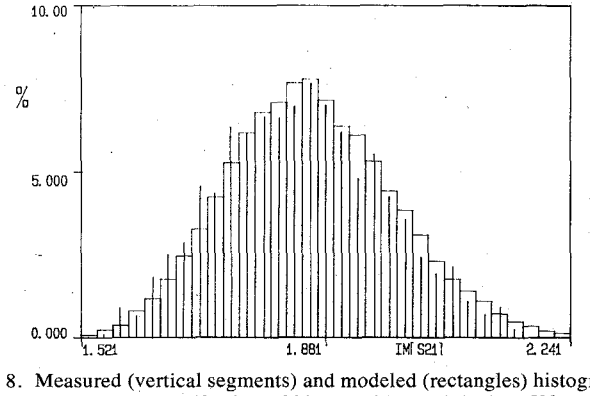

Fig. 8. Measured (vertical segments) and modeled (rectangles) histograms of the imaginary part of $S21$ for a 300 μm wide FET device (Vds = 5 V Ids = $Idss/2$).

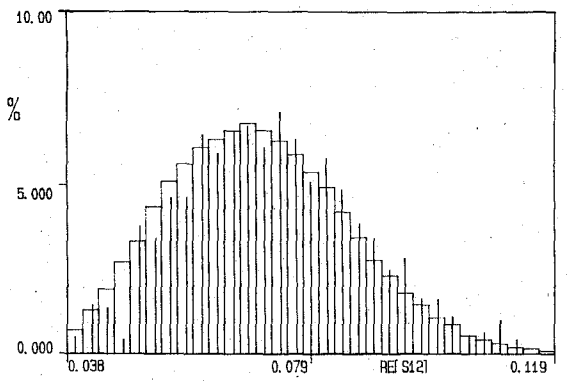

Fig. 9. Measured (vertical segments) and modeled (rectangles) histograms of the real part of $S12$ for a 300 μm wide FET device (Vds = 5 V Ids = $Idss/2$).

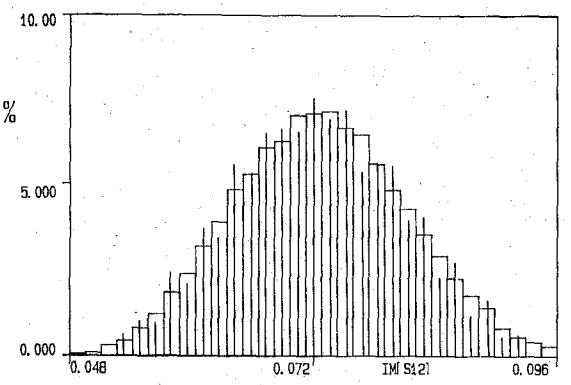

Fig. 10. Measured (vertical segments) and modeled (rectangles) histograms of the imaginary part of $S12$ for a 300 μm wide FET device (Vds = 5 V Ids = $Idss/2$).

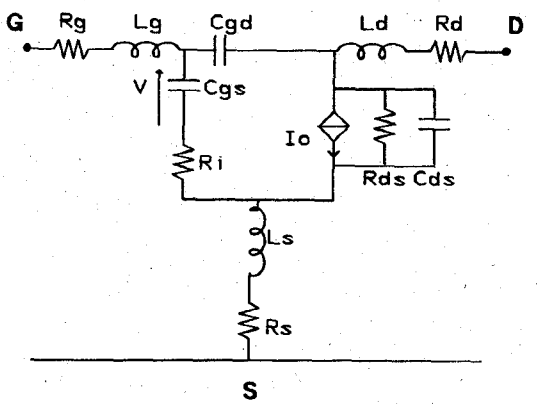

Fig. 11. FET small signal equivalent circuit.

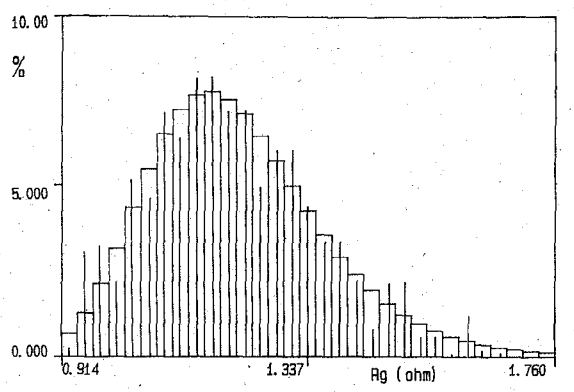

Fig. 12. Measured (vertical segments) and modeled (rectangles) histograms of the gate resistance Rg for a 300 μm wide FET device (Vds = 5 Ids = $Idss/2$).

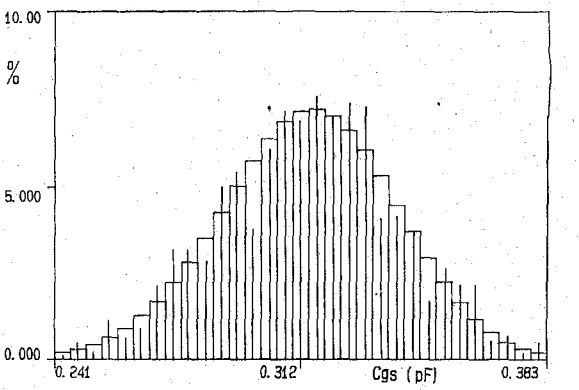

Fig. 13. Measured (vertical segments) and modeled (rectangles) histograms of the gate to source capacitance Cgs for a 300 μm wide FET device (Vds = 5 V Ids = $Idss/2$).

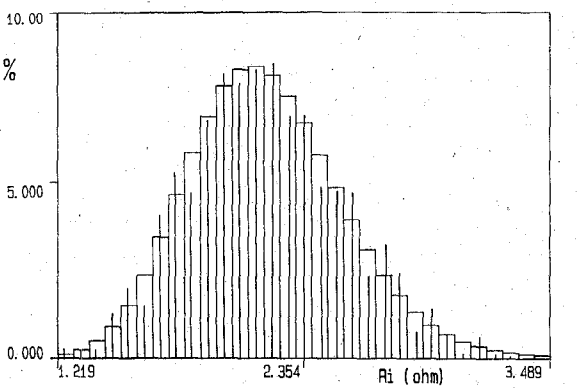

Fig. 14. Measured (vertical segments) and modeled (rectangles) histograms of the resistance Ri for a 300 μm wide FET device (Vds = 5 V Ids = $Idss/2$).

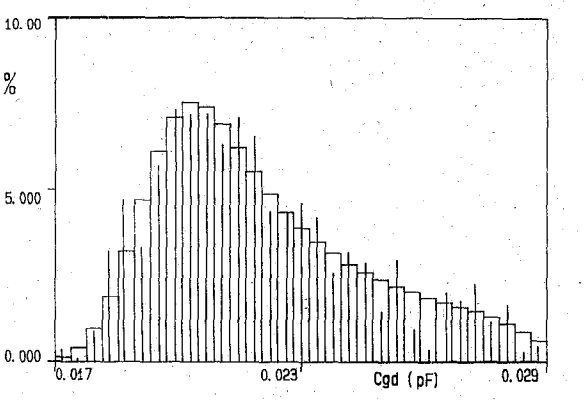

Fig. 15. Measured (vertical segments) and modeled (rectangles) histograms of the gate to drain capacitance Cgd for a 300 μm wide FET device (Vds = 5 V Ids = $Idss/2$).

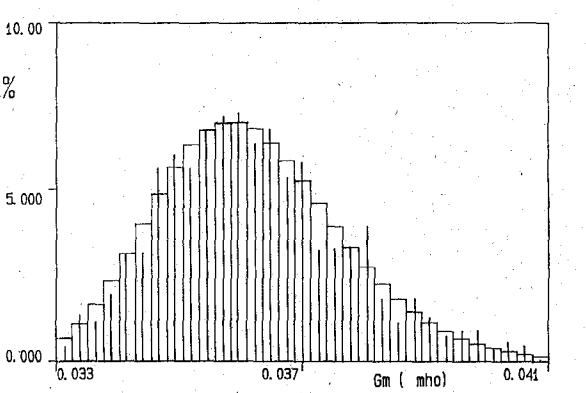

Fig. 16. Measured (vertical segments) and modeled (rectangles) histograms of the transconductance gm for a 300 μm wide FET device (Vds = 5 V Ids = $Idss/2$).

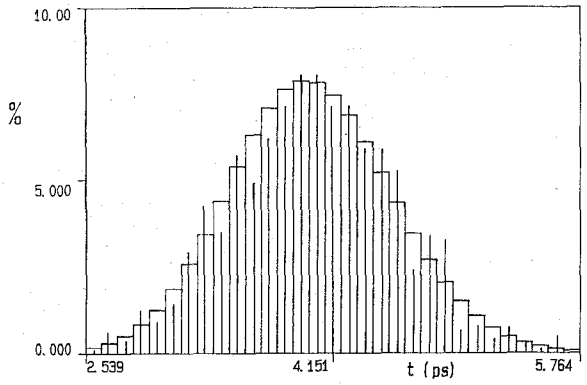

Fig. 17. Measured (vertical segments) and modeled (rectangles) histograms of the delay time t for a 300 μm wide FET device (Vds = 5 V Ids = $Idss/2$).

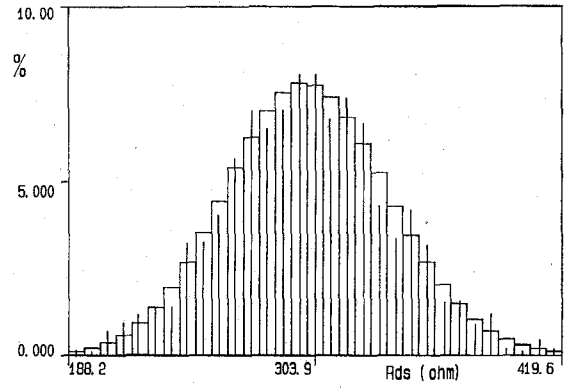

Fig. 18. Measured (vertical segments) and modeled (rectangles) histograms of the drain to source resistance Rds for a 300 μm wide FET device (Vds = 5 V Ids = $Idss/2$).

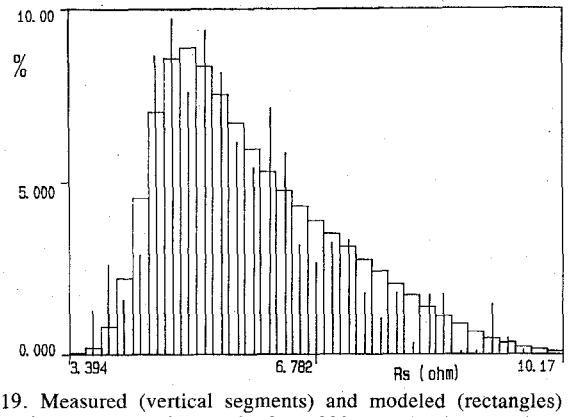

Fig. 19. Measured (vertical segments) and modeled (rectangles) histograms of the source resistance Rs for a 300 μm wide FET device (Vds = 5 V Ids = $Idss/2$).

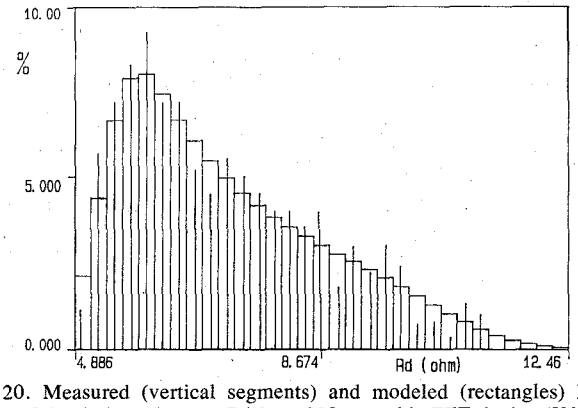

Fig. 20. Measured (vertical segments) and modeled (rectangles) histograms of the drain resistance Rd for a 300 μm wide FET device (Vds = 5 V Ids = $Idss/2$).

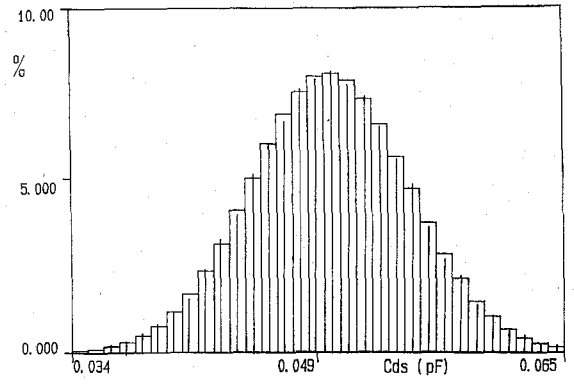

Fig. 21. Measured (vertical segments) and modeled (rectangles) histograms of the drain to source capacitance Cds for a 300 μm wide FET device (Vds = 5 V Ids = $Idss/2$).

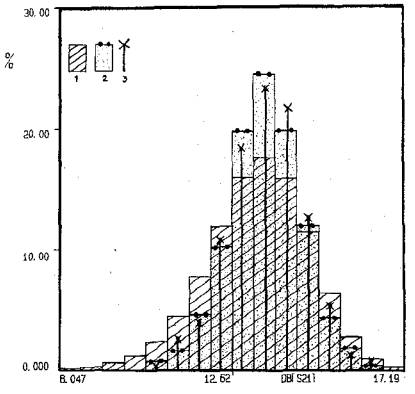

Fig. 22. MMIC S21 histograms using uncorrelated E. C. parameters (1), our model (2) and as they result from experiment (3).

considered as uncorrelated, was Yp = 69%. A much more realistic result (Yp = 90.6%) was obtained from the FET model in the appendix. Fig. 22 shows the circuit S21 histogram (1) calculated assuming as uncorrelated the FET equivalent circuit parameters, the histogram (2) calculated with the FET model in appendix and, finally the experimental one (3). Very accurate Yp evaluations were also obtained from the model for other routinely produced MMICs [37], [39].

V. Conclusions

By making reference to a specific development philosophy, a critical analysis has been made of the state of the art design criteria and tools for MMIC to be produced in large quantities. The different kinds of yields, related to the manufacturing procedure, have been examined and the relevant evaluation criteria discussed. Various weaknesses of the information usually available from foundries have been outlined.

The results have been reported of a systematic functional yield analysis we performed on a large number of monolithic circuit components. A statistically meaningful and self consistent data base, using both FET S and equivalent circuit parameters, has been given for a standard 0.5 μm MMIC process.

Useful information and references for foundry customers have also been given. Finally, the possibility has been demonstrated of accurately evaluating the param-

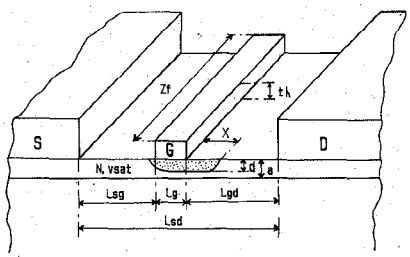

Fig. 23. Sketch of the considered FET structure.

TABLE III
PROCESS RELATED FLUCTUATING PARAMETERS

Parameter	Mean Value	Stand. Dev.	Units
Peak doping density N	2.55E17	0.063E17	cm^{-3}
Active layer thickness a	0.148	0.0017	μm
Gate length Lg	0.5	0.05	μm
Gate to source distance Lsg	1	0.18	μm
Saturated drift velocity $vsat$	0.9E7	0.047E7	cm/s
Built-in voltage Vbo	0.75	0.038	V

TABLE IV
ANALYTICAL RELATIONSHIPS

$N' = 0.82 * N$	
$Rse = K1 * Lsg/(q * N' * u * a * Z)$	$K1$: fitting constant q: electron charge u: free space permeability Z: total gate width
$Rde = K2 * Lgd/(q * N' * u * a * Z)$	$K2$: fitting constant
$d = [2 * K * (Vbo - Vgsi)/(9 * N')]$ ** 1/2	K: GaAs dielectric constant $Vgsi$: intrinsic gate to source voltage
$Ids = q * N' * vsat * Z * (a - d)$	
$X = (Vdg + Vbo) * \{2 * K/[q * N' * (Vbo - Vgs)]\}$ ** 1/2	Vgs: gate to source voltage
$t = K3 * Lg/vsat$	t: delay time-K3 fitting constant
$Cgdo = K * Z/(1 + 2 * X/Lg)$	

etric yields of MMIC's we produce in large quantities by using a small set of really uncorrelated process dependent parameters and of a physically based FET model, semiempirically centered on the used technology.

APPENDIX
THE SEMIEMPIRICAL PHYSICALLY BASED MODEL

This model is not a complete and flexible tool for representing the device behaviour for any bias condition. It is here considered just for proving that very accurate parametric yield evaluations can be obtained by using a physically based FET model semiempirically centered on the fabrication process. For this reason it is optimized for taking into account the device behavior around a fixed bias condition (which is always the same for all the devices of the MMIC's mentioned in paragraph IV). On the other hand the MMIC manufacturers, which are interested in our basic approach, can choose in a wide literature [5], [40], [41], [42], [43] more flexible physically based FET models.

Fig. 23 gives a sketch of the device structure and Table III reports the process related fluctuating parameters we consider. The source and drain resistances, *Rs* and *Rd*, are considered as the sum of a contact resistance *Rc* and the resistance of the extrinsic semiconductor regions (*Rse* and *Rde*, respectively). Rc is modeled as a function of *N* (peak doping density), a (see Fig. 23) and *Z* (total gate width) as given in [44] assuming, for a more close evaluation of the measured PCM contact resistances, a fitting factor = 2 (instead of 2.1). *Rse* and *Rde* are modeled as in [5] using the Table IV expressions. Similarly, the channel current *Ids*, the depletion thickness *d* and the amplitude of the depleted region toward the drain *X* were assumed as in [5] and Table IV. The transconductance *gm* and the gate to source capacitance *Cgs* are modeled as in [45] assuming the fitting factors .0185 and .32, respectively.

The gate to drain capacitance Cgd is considered as the sum of the proximity on Cgdp [5], [16], [46], [47], [48] and the depletion one Cgdo ([5] and Table IV), the last one being weighted for fitting the measured mean values. Inductances *Lg*, *Ld* and *Ls* have no relevance in the design of the MMIC's, mentioned in paragraph IV, so their fluctuations are not considered.

The *Rds* behavior around the bias condition was experimentally determined as in [48]. Its dependence on *Lg* and *N* was also assumed as in [49].

Cds was considered as an independent gaussian parameter, having the mean value and standard deviation of the data extracted from measurements.

ACKNOWLEDGMENT

The authors are indebted to Dr. Salvatore Iannazzo of Alcatel-Telettra and to the MTT Reviewers for useful suggestions which significantly contributed to the clarity of the paper.

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